# 8 PCB Layout Guideline

Line width of high current path such as power input and output need to be widened to reduce line impedance, voltage drop and loss.

- Line width of DCDC input and output: >=150mil
- Line width of output depends on load current.
- The DCDC feedback lines need to be well shielded to avoid parallel layout with high-frequency signals on the same layer such as LX.
- Inductors of DCDCs are close to PMIC and output capacitors are close to inductors.
- Input capacitors of DCDCs are close to input pins(VIN1/VIN2/VIN3) and the input power enters the input pins after passing through the input capacitors. Refer to the following figure(input power -> via -> capacitor -> input pin).

Figure 8-1 PCB reference