6 Video Output Interfaces

6.1 eDP1.3

6.1.1 Overview

The Embedded Display Port (eDP) is a standard protocol in the digital display field. It is completely compatible with DP and consists of main link, auxiliary channel, and hot plugging.

The eDP includes the following features:

- Up to 2.5K@60fps
- 1-lane, 2-lane, or 4-lane transmission, up to 2.7 Gbps/lane
- Video formats: RGB, YCbCr4:4:4, and YCbCr4:2:2
- Color depth: 8-bit and 10-bit per channel
- Supports I2S interface
  - Supports mono sound, stereo sound, and 7.1 surround sound
  - Maximum sampling rate: 192 kHz
- Full link training
- Hot plug detection
- AUX channel
  - Maximum working frequency: 1MHz
  - Adopts Manchester-II encoding
- Clock spread spectrum
- Programmable voltage swing and pre-emphasis
- Embedded ESD

6.1.2 Functional Descriptions

6.1.2.1 External Signals

The following table describes the external I/O signals of the eDP module.

Table 6-1 eDP External Signals

Signal Name	Description	Type
EDP-AUXN	AUX channel Negative Input/Output	A I/O
EDP-AUXP	AUX channel Positive Input/Output	A I/O

Signal Name	Description	Type
EDP-HPD	Hot Plug Detection Signal	AI
EDP-REXT	eDP External Reference Resistor	AO
EDP-TX0N	eDP Negative Output of Data Channel0	AO
EDP-TX0P	eDP Positive Output of Data Channel0	AO
EDP-TX1N	eDP Negative Output of Data Channel1	AO
EDP-TX1P	eDP Positive Output of Data Channel1	AO
EDP-TX2N	eDP Negative Output of Data Channel2	AO
EDP-TX2P	eDP Positive Output of Data Channel2	AO
EDP-TX3N	eDP Negative Output of Data Channel3	AO
EDP-TX3P	eDP Positive Output of Data Channel3	AO
VCC18-EDP	1.8V Analog Supply	P
VDD09-EDP	0.9V Digital Supply	P

6.1.2.2 PLL Configuration

Allwinner eDP TX IP contains a core PLL to generate core clock and high speed half-rate bit clock required for normal operation from the reference clock. If the additional pixel PLL is included, it can generate the pixel clock for controller from the reference clock.

- Core PLL VCO Clock

The frequency of core PLL VCO clock is controlled by pre-div divider (corepll_prediv [5:0], 0x0180[13:8]) and feedback divider (corepll_fbdiv [11:0], 0x0180[19:16]and 0x0180[31:24]). The pre-PLL VCO frequency is calculated as:

fcorevco = fref / corepll_prediv [5:0] * corepll_fbdiv [11:0]

For fractional operation, the fractional divider (corepll_frac [23:0], 0x0184 [7:0], 0x0184 [15:8] and 0x0184 [23:16]) should be turned on by setting the fractional divider control register (corepll_frac_pd [1:0], 0x0180[5:4]) to 2'b00. The core PLL VCO frequency is calculated as:

fcorevco = fref / corepll_prediv [5:0] * (corepll_fbdiv [11:0] +corepll_frac [23:0]/224)

- Bit Clock

The frequency of bit clock should be half of the channel data rate and is controlled by post-div divider (corepll_postdiv [1:0], 0x0188[3:2]). The frequency of bit clock is calculated as:

fbitclk = fcorevco / corepll_postdiv [1:0]

- Core Clock

The frequency of core clock is calculated as:

fcoreclk = fbitclk / 10

- Pixel PLL VCO Clock

The frequency of pixel PLL VCO clock is controlled by pre-div divider (pixelpll_prediv [5:0], 0x00A1 [5:0]) and feedback divider (pixelpll_fbdiv [11:0], 0x0190 [19:16] and 0x0190 [31:24]). The pixel PLL VCO frequency is calculated as:

fpixelvco = fref / pixelpll_prediv [5:0] * pixelpll_fbdiv [11:0]

For fractional operation, the fractional divider (pixelpll_frac [23:0], 0x019C [7:0], 0x019C [15:8] and 0x019C [23:16]) should be turned on by setting the fractional divider control register (pixelpll_frac_pd [1:0], 0x0190[5:4]) to 2'b00. The pixel PLL VCO frequency is calculated as:

fpixelvco = fref / pixelpll_prediv [5:0] * (pixelpll_fbdiv [11:0] +pixelpll_frac [23:0]/2^{24})

- Pixel Clock

The frequency of pixel clock is controlled by pixel clock divider a (pixelpll_pclkdiva [4:0], 0x0194 [4:0]), divider b (pixelpll_pclkdivb [1:0], 0x0194[9:8]) and divider c (pixelpll_pclkdivc [4:0], 0x0194 [20:16]). When pixelpll_pclkdiva [4:0] is set to be 5'h01, the frequency of pixel clock is calculated as:

fpclk = fpixelvco / (2*pixelpll_pclkdivb [1:0] *pixelpll_pclkdivc [4:0])

When pixelpll_pclkdiva [4:0] is not set to be 5'b01, the frequency of pixel clock is calculated as:

fpclk = fpixelvco / (2*pixelpll_pclkdiva [4:0] * pixelpll_pclkdivc [4:0])

NOTE

- The VCO running frequency should be kept in the range from 1 GHz to 3 GHz for core PLL and pixel PLL.
- PLL should be power down before configuration.

Table below gives the recommended core PLL configuration with 24MHz reference clock for typical link rates.

Table 6-2 Recommended Core PLL Configuration with 24MHz Reference Clock

Link Rate	1.62G	2.7G
core PLL VCO	1.62GHz	2.7GHz
bit clock	0.81GHz	1.35GHz
core clock	81MHz	135MHz
24MHz reference clock		
corepll_prediv[5:0]	6'h02	6'h02
corepll_fbdiv[11:0]	12'h087	12'h0e1
corepll_postdiv[1:0]	2'b01	2'b01
corepll_frac_pd[1:0]	2'b11	2'b11
corepll_frac[23:0]	24'b0	24'b0

Table below gives the recommended pixel PLL configuration with 24MHz reference clock for typical video formats.

Table 6-3 Recommended Pixel PLL Configuration with 24MHz Reference Clock

Video Format	720P/60	1080P/60	2160P/30
pixel PLL VCO	2.376GHz	2.376GHz	2.376GHz
pixel clock	74.25MHz	148.5MHz	297MHz
24MHz reference clock			
pixelpll_prediv[5:0]	6'h01	6'h01	6'h01
pixelpll_fbdiv[11:0]	12'h063	12'h063	12'h063
pixelpll_pclkdiva[4:0]	5'h01	5'h01	5'h01
pixelpll_pclkdivb[1:0]	2'b01	2'b01	2'b01
pixelpll_pclkdivc[4:0]	5'h08	5'h04	5'h02
pixelpll_frac_pd[1:0]	2'b11	2'b11	2'b11
pixelpll_frac[23:0]	24'b0	24'b0	24'b0

6.1.2.3 Termination Configuration

In order to improve the signal quality, the termination resistance should match the impedance of PCB trace to minimize reflection. The differential characteristic impedance of differential pair trance on PCB is typical 100Ω. Thus the differential termination resistance of the receiver is preferred to be 100Ω around.

The termination resistance could be manually set by writing the differential termination resistance control registers (rtm [5:0], 0x01C4[5:0]/0x01C4[13:8]/0x01C4[21:16]/0x01C4[29:24]) with reference value for 4 data channels and AUX channel, respectively. The reference value for TT corner is calculated as:

RT = 4000 / rtm [5:0]

For example, if rtm [5:0] is set to 6'h28 and the decimal value is 40, the differential termination resistance will be 100Ω for TT corner. If rtm [5:0] is set to 6'h00, the termination resistance will be turned off. However, the termination resistance value varies along with the process variation.

Allwinner eDP TX IP also employs a resistance calibration mechanism to eliminate the process variation. The resistance calibration compares the termination resistor with the off-chip reference resistor, and adjusts its value to the target value set by calibration control register (rcal_sel [1:0], 0x01C0[26:25]) with insignificant error. The calibration result will be stored in calibration result register (rcal_val [5:0], 0x01C0[5:0]). After calibration, the transmitter termination resistance will be configured according to the calibration result.

The configuration method for termination resistance is controlled by the calibration bypass register (rcal_byp, 0x01C0[15]). If the termination resistance is desired to be set with the manual method, the resistance calibration should be bypassed.

The termination resistance calibration is configured as follow:

Step 1 configure the resistance calibration clock divider (0x01C0[14:8] and 0x01C0[23:16]) to set the clock frequency to be 100KHz around. For example, if the system clock is 100MHz, write 15'd1000 to the divider register.

Step 2 configure the resistance calibration target value (0x01C0[26:25]). For example, if 100Ω differential termination resistance is desired, write 2'b00 to register 0x01C0[26:25].

Step 3 configure the calibration bypass register (0x01C0[15]) to start the resistance calibration by writing 1'b1 to 0x01C0[15] firstly and then writing 1'b0 to register 0x01C0[15]. A falling edge of 0x01C0[15] will trigger the startup of the automatic resistance calibration. After calibration is done, the termination resistance of data channels and AUX channel will be configured according to the calibration result.

6.1.2.4 Transmitter Configuration

The transmitter in each data channel adopts 3-tap FFE (Feed Forward Equalizer) to compensate the channel loss, including the pre-cursor tap, main cursor tap and post-cursor tap. The pre-cursor tap and the post-cursor tap serve as the pre-emphasis.

The output levels of above 3 taps are all programmable and controlled by the driver current bias (Ibias). Ibias can be adjusted by current bias control register (isel [3:0], 0x01A8[3:0] 0x01A8[7:4] 0x01A4[27:24] and 0x01A4[31:28]) and is calculated as:

Ibias = 160uA + 40uA * isel [3:0]

There are also independent registers to adjust the levels of 3 taps, respectively.

The main cursor tap could be adjusted by registers output voltage level control registers (mainsel [4:0], 0x01AC[12:8]/0x01AC[4:0]/0x01A8[28:24]/0x01A8[20:16]) for 4 TMDS channels, respectively, and the output current level is calculated as:

Imain = Ibias * mainsel [4:0]

The pre-cursor tap could be adjusted by pre-cursor pre-emphasis level control registers (presel [2:0], 0x01B0[6:4]/0x01B0[2:0]/0x01B0[14:12]/0x01B0[10:8]) for 4 TMDS data channels, respectively, and the output current level is calculated as:

Ipre = Ibias * presel [2:0]

The post-cursor tap could be adjusted by post-cursor pre-emphasis level control registers (postsel [3:0], 0x01AC [23:20]/0x01AC [19:16]/0x01AC [31:28]/0x01AC [27:24]) for 4 TMDS channels, respectively, and the output current level is calculated as:

Ipost = Ibias * postsel [3:0]

The pre-cursor pre-emphasis level is calculated as:

Lpre = 20 * log [(Imain + Ipre) / (Imain – Ipre)]

The post-cursor pre-emphasis level is calculated as:

Lpost = 20 * log [(Imain + Ipost) / (Imain – Ipost)]

The combinations of different levels of 3 taps result in different transmitter eye and output voltage levels for different data pattern. The pre-emphasis levels should be carefully adjusted according to the actual condition to minimize the ISI introduced by the TX end. The following table gives the recommended transmitter configuration for different data rates.

Table 6-4 Recommended Transmitter Configuration for Different Data Rates

Register	Level	1.62Gbps	2.7Gbps
isel[3:0]	Voltage Swing Level 0	4'b0000	4'b0000
	Voltage Swing Level 1	4'b0010	4'b0010
	Voltage Swing Level 2	4'b0100	4'b0100
	Voltage Swing Level 3	4'b0110	4'b0110
mainsel[4:0]		5'b11111	5'b11111
postsel[3:0]	Pre-emphasis Level 0	4'b0000	4'b0000
	Pre-emphasis Level 1	4'b0001	4'b0001
	Pre-emphasis Level 2	4'b0010	4'b0010
	Pre-emphasis Level 3	4'b0011	4'b0011
presel[2:0]		3'b000	3'b000

6.1.2.5 SSC Configuration

Allwinner eDP TX IP contains SSC function for data channel to deal with possible EMI problem. The features the SSC modulation are listed as follow:

- Support down spread and center spread modulation.
- Support 3-bit programmable modulation depth from 500ppm to 32000ppm.
- Support default triangular wave and programmable wave modulation.
- Support adjustable modulation frequency.

The SSC modulation is configured as follows:

Step 1 Configure the modulation mode control register (0x0180[20]) to select down spread or center spread.

Step 2 Configure the modulation frequency control register (0x0188[27:24]) to select SSC modulation frequency.

Step 3 Configure the modulation amplitude control register (0x0188[30:28]) to select SSC modulation amplitude.

Step 4 Configure the fractional PLL enable register (0x0180[5:4]) to 2'b00.

Step 5 Configure the SSC modulation enable register (0x0180[21]) to 1'b0.

The SSC modulation frequency is calculated as:

$f_{ssc} = f_{ref}$ /corepll_prediv[5:0]/128/decimal value of 0x0188[27:24]

The default setting results in down spread SSC modulation with 31.25KHz frequency and 4000ppm amplitude with 24MHz reference clock.

6.1.3 Register List

Module Name	Base Address
EDP	0x0572_0000

Register Name	Offset	Description
EDP_HPD_SCALE	0x0018	EDP HPD Scale Register
EDP_RST	0x001C	EDP Reset Register
EDP_HPD_EVENT	0x0080	HPD Event Status Register
EDP_HPD_INT	0x0084	Enable Hpd Plug Interrupt Register
EDP_HPD_PLUG	0x0088	HPD Plug Event Register
EDP_HPD_EN	0x008C	HPD Plug EN Register
EDP_CAPACITY	0x0100	Capacity Register
EDP_ANA_PLL_FBDIV	0x0180	CORE Pll Fbdiv Register
EDP_ANA_PLL_FRAC	0x0184	Core Pll Frac Register
EDP_ANA_PLL_POSDIV	0x0188	Core Pll Postdiv Register
EDP_ANA_PIXELPLL_FBDIV	0x0190	Pixel Pll Feedback Divide Register
EDP_ANA_PIXELPLL_DIV	0x0194	Pixel Pll Divider Register
EDP_ANA_PIXELPLL_FRAC	0x019C	Pixel Pll Frac Register
EDP_TX32_ISEL_DRV	0x01A4	Lane 32 Current Bias Control Register
EDP_TX_MAINSEL	0x01A8	Output Voltage Control Register
EDP_TX_POSTSEL	0x01AC	Post-cursor Pre-Emphasis Register
EDP_TX_PRESEL	0x01B0	Pre-cursor Pre-Emphasis Register
EDP_TX_RCAL_SEL	0x01C0	The Resistance Calibration Register
EDP_VIDEO_STREAM_EN	0x0200	Video_Stream Enable Register
EDP_SYNC_POLARITY	0x020C	Polarity of Hsync and Vsync Register
EDP_HACTIVE_BLANK	0x0210	H acitve and Blank Register
EDP_VACTIVE_BLANK	0x0214	V acitve and Blank Register
EDP_HWIDTH_FRONT_PORCH	0x0218	Hs Width and H Front Porch Register
EDP_VWIDTH_FRONT_PORCH	0x021C	Vs Width and V Front Porch Register
EDP_FRAME_UNIT	0x0220	Transfer Unit Register
EDP_SYNC_START	0x0224	Vstart and Hstart Register
EDP_MSA_MISC0	0x0228	MSA Miscellaneous0 Field Register
EDP_MSA_MISC1	0x022C	MSA Miscellaneous1 Field Register
EDP_HBLAN_LINK_CYC	0x0230	Hblank Link CYC Register
EDP_AUDIO	0x0300	Audio Register

6.2 MIPI DSI

The Display Serial Interface is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.02 and a D-PHY module which is compliance with MIPI DPHY specification V1.1.

The MIPI DSI includes the following features:

- Compliance with MIPI DSI V1.02
- Up to 1.5 Gbit/s for each lane
- Supports 4-lane MIPI DSI, up to 1280 x 720@60fps and 1920 x 1200@60fps
- Supports 4+4-lane MIPI DSI, up to 2560 x 1600@60fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Continuous and non-continuous lane clock modes
- Generic commands support bidirectional communication in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes
- Supports hardware checksum

6.3 TCON LCD

6.3.1 Overview

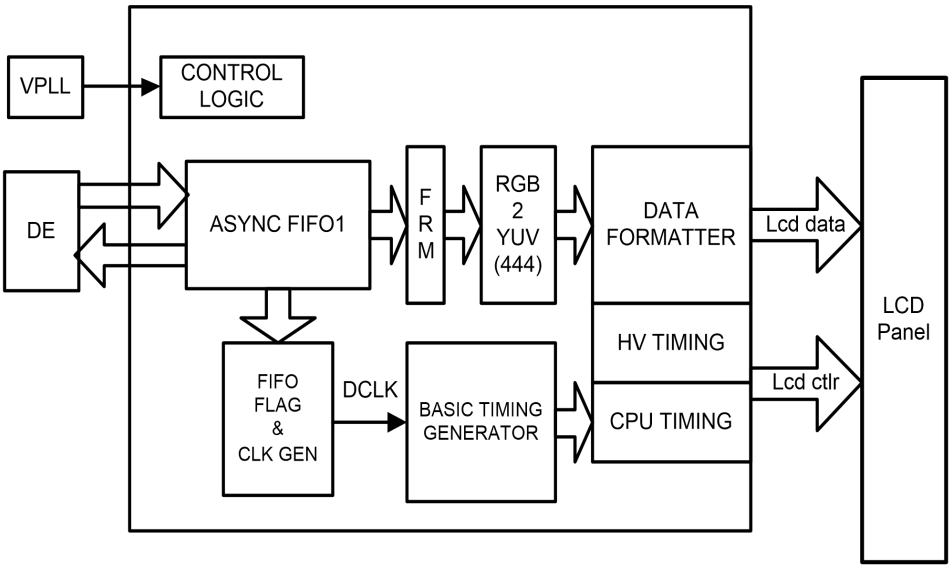
The Timing Controller_LCD (TCON_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- Two TCON LCD controllers: TONC_LCD0 and TCON_LCD1
- TCON_LCD0 supports the following
  - Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
  - Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
  - Supports LVDS interface with dual link, up to 1920 x 1080@60fps
  - Supports LVDS interface with single link, up to 1366 x 768@60fps
  - Dither function for RGB888, RGB666, and RGB565
  - Supports i8080 interface, up to 800 x 480@60fps
  - Supports BT.656 interface for NTSC and PAL
  - Supports MIPI DSI interface with dual link, up to 2560x1600@60fps
  - Supports MIPI DSI interface with single link, up to 1920x1200@60fps
- TCON_LCD1 supports MIPI DSI interface with single link, up to 1920x1200@60fps

6.3.2 Block Diagram

Figure 6-1 TCON_LCD Block Diagram



6.3.3 Functional Description

6.3.3.1 External Signals

The following table describes the external I/O signals of LCD and LVDS.

Table 6-5 TCON_LCD External Signals

Signal Name	Description	Type
LCD0-D[23:0]	LCD Data Input/Output	I/O
LCD0-CLK	LCD Clock The pixel data are synchronized by this clock	O
LCD0-VSYNC	LCD Vertical Sync It indicates one new frame	O
LCD0-HSYNC	LCD Horizontal Sync It indicates one new scan line	O
LCD0-DE	LCD Data Output Enable	O
LCD0-TRIG	LCD0 Sync It is input from peripherals for sync	I
LCD1-TRIG	LCD1 Sync It is input from peripherals for sync	I
LVDS0-D[3:0]N	LVDS0 Negative Port of Data Channel [3:0]	AO
LVDS0-D[3:0]P	LVDS0 Positive Port of Data Channel [3:0]	AO
LVDS0-CKN	LVDS0 Negative Port of Clock	AO
LVDS0-CKP	LVDS0 Positive Port of Clock	AO
LVDS1-D[3:0]N	LVDS1 Negative Port of Data Channel [3:0]	AO
LVDS1-D[3:0]P	LVDS1 Positive Port of Data Channel [3:0]	AO
LVDS1-CKN	LVDS1 Negative Port of Clock	AO
LVDS1-CKP	LVDS1 Positive Port of Clock	AO

For parallel RGB, the data of LCD is high-aligned. The correspondence is as follows.

Table 6-6 The Correspondence between LCD and RGB

LCD I/O	Parallel RGB I/O		
	RGB565	RGB666	RGB888
LCD0-D23	R4	R5	R7
LCD0-D22	R3	R4	R6
LCD0-D21	R2	R3	R5
LCD0-D20	R1	R2	R4
LCD0-D19	R0	R1	R3
LCD0-D18	-	R0	R2
LCD0-D17	-	-	R1
LCD0-D16	-	-	R0
LCD0-D15	G5	G5	G7

LCD I/O	Parallel RGB I/O		
	RGB565	RGB666	RGB888
LCD0-D14	G4	G4	G6
LCD0-D13	G3	G3	G5
LCD0-D12	G2	G2	G4
LCD0-D11	G1	G1	G3
LCD0-D10	G0	G0	G2
LCD0-D9	-	-	G1
LCD0-D8	-	-	G0
LCD0-D7	B4	B5	B7
LCD0-D6	B3	B4	B6
LCD0-D5	B2	B3	B5
LCD0-D4	B1	B2	B4
LCD0-D3	B0	B1	B3
LCD0-D2	-	B0	B2
LCD0-D1	-	-	B1
LCD0-D0	-	-	B0

The multiplex relationship among LCD, LVDS, and DSI is shown as follows.

Table 6-7 The Correspondence among LCD, LVDS, and DSI.

LCD I/O	LVDS I/O	DSI I/O
LCD0-D0	/	/
LCD0-D1	/	/
LCD0-D2	LVDS0-D0P	DSI0-D0P
LCD0-D3	LVDS0-D0N	DSI0-D0N
LCD0-D4	LVDS0-D1P	DSI0-D1P
LCD0-D5	LVDS0-D1N	DSI0-D1N
LCD0-D6	LVDS0-D2P	DSI0-CKP
LCD0-D7	LVDS0-D2N	DSI0-CKN
LCD0-D8	/	/
LCD0-D9	/	/
LCD0-D10	LVDS0-CKP	DSI0-D2P
LCD0-D11	LVDS0-CKN	DSI0-D2N
LCD0-D12	LVDS0-D3P	DSI0-D3P
LCD0-D13	LVDS0-D3N	DSI0-D3N
LCD0-D14	LVDS1-D0P	DSI1-D0P
LCD0-D15	LVDS1-D0N	DSI1-D0N
LCD0-D16	/	/
LCD0-D17	/	/
LCD0-D18	LVDS1-D1P	DSI1-D1P
LCD0-D19	LVDS1-D1N	DSI1-D1N
LCD0-D20	LVDS1-D2P	DSI1-CKP

LCD I/O	LVDS I/O	DSI I/O
LCD0-D21	LVDS1-D2N	DSI1-CKN
LCD0-D22	LVDS1-CKP	DSI1-D2P
LCD0-D23	LVDS1-CKN	DSI1-D2N
LCD0-CLK	LVDS1-D3P	DSI1-D3P
LCD0-DE	LVDS1-D3N	DSI1-D3N
LCD0-HSYNC	/	/
LCD0-VSYNC	/	/

6.3.3.2 Clock Sources

The following table describes the clock sources of TCON_LCD.

Table 6-8 TCON_LCD Clock Sources

Clock sources	Description	Module
PLL_VIDEO0(3x)	By default, PLL_VIDEO0(4x) is 1188 MHz, PLL_VIDEO0(3x) is 792MHz.	CCU
PLL_VIDEO0(4x)		
PLL_VIDEO1(3x)	By default, PLL_VIDEO1(4x) is 1188 MHz, PLL_VIDEO1(3x) is 792MHz.	
PLL_VIDEO1(4x)		
PLL_VIDEO2(4x)	By default, PLL_VIDEO2(4x) is 1188 MHz.	
PLL_VIDEO3(4x)	By default, PLL_VIDEO3(4x) is 1188 MHz.	
PLL_PERI0(2x)	By default, PLL_PERI0(2x) is 1.2 GHz.	

6.3.3.3 Control signal and data port mapping

		SYNC RGB				YUV		DC	CPU Cmd	CPU 18-bit	CPU 18-bit							CPU 16-bit	CPU 18-bit			CPU 16-bit		CPU 18-bit		LVDS		DSI	
External I/O	Internal pin	Para	Serial RGB			BT656	BT601	YUV422		256K	256K							64K	256K			64K		256K		Single Link		DSI 0	DSI1
			1st	2nd	3rd						1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2nd	1st	2nd	LVDS0	LVDS1		
LCD0_VSYNC	IO0	VSYNC					VSYNCC	VSYNC	CS																				
LCD0_HSYNC	IO1	HSYNC					HSYNC		RD																				
LCD0_CLK	IO2	DCLK				PCLK	DCLK	DCLK	WR																		D3N		D3N
LCD0_DE	IO3	DE					DE	HSYNC	RS																		D3P		D3P
LCD0_D23	D23	R7							D23	R5	R5	B5	G5	R5		R5	B5	R4									CKN		D2N
LCD0_D22	D22	R6							D22	R4	R4	B4	G4	R4		R4	B4	R3									CKP		D2P
LCD0_D21	D21	R5							D21	R3	R3	B3	G3	R3		R3	B3	R2									D2N		CKN
LCD0_D20	D20	R4							D20	R2	R2	B2	G2	R2		R2	B2	R1									D2P		CKP
LCD0_D19	D19	R3							D19	R1	R1	B1	G1	R1		R1	B1	R0									D1N		D1N
LCD0_D18	D18	R2							D18	R0	R0	B0	G0	R0		R0	B0	G5									D1P		D1P
LCD0_D17	D17	R1							D17																		D0N		D0N
LCD0_D16	D16	R0							D16																		D0P		D0P
LCD0_D15	D15	G7							D15	G5								G4											
LCD0_D14	D14	G6							D14	G4								G3											
LCD0_D13	D13	G5							D13	G3																D3N		D3	
LCD0_D12	D12	G4	D71	D72	D73	D7	D7	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2	D3P		D3P	
LCD0_D11	D11	G3	D61	D62	D63	D6	D6	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1	CKN		D2	
LCD0_D10	D10	G2	D51	D52	D53	D5	D5	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0	CKP		D2P	
LCD0_D9	D9	G1							D9																				
LCD0_D8	D8	G0							D8																				
LCD0_D7	D7	B7	D41	D42	D43	D4	D4	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5	D2N		CK	
LCD0_D6	D6	B6	D31	D32	D33	D3	D3	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4	D2P		CK	
LCD0_D5	D5	B5	D21	D22	D23	D2	D2	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3	D1N		D1	
LCD0_D4	D4	B4	D11	D12	D13	D1	D1	D1	D4	B2								B1				G4	B1	G5	B2	D1P		D1P	
LCD0_D3	D3	B3	D01	D02	D03	D0	D0	D0	D3	B1								B0				G3	B0	G4	B1	D0N		D0	
LCD0_D2	D2	B2							D2	B0														G3	B0	D0P		D0P	
LCD0_D1	D1	B1							D1																				
LCD0_D0	D0	B0							D0																				

6.3.3.4 HV interface (Sync+DE mode)(Only for TCON_LCD0)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

Its signals are defined as:

Table 6-9 HV Panel Signals

Signal Name	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
DE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

Figure 6-2 HV Interface Vertical Timing

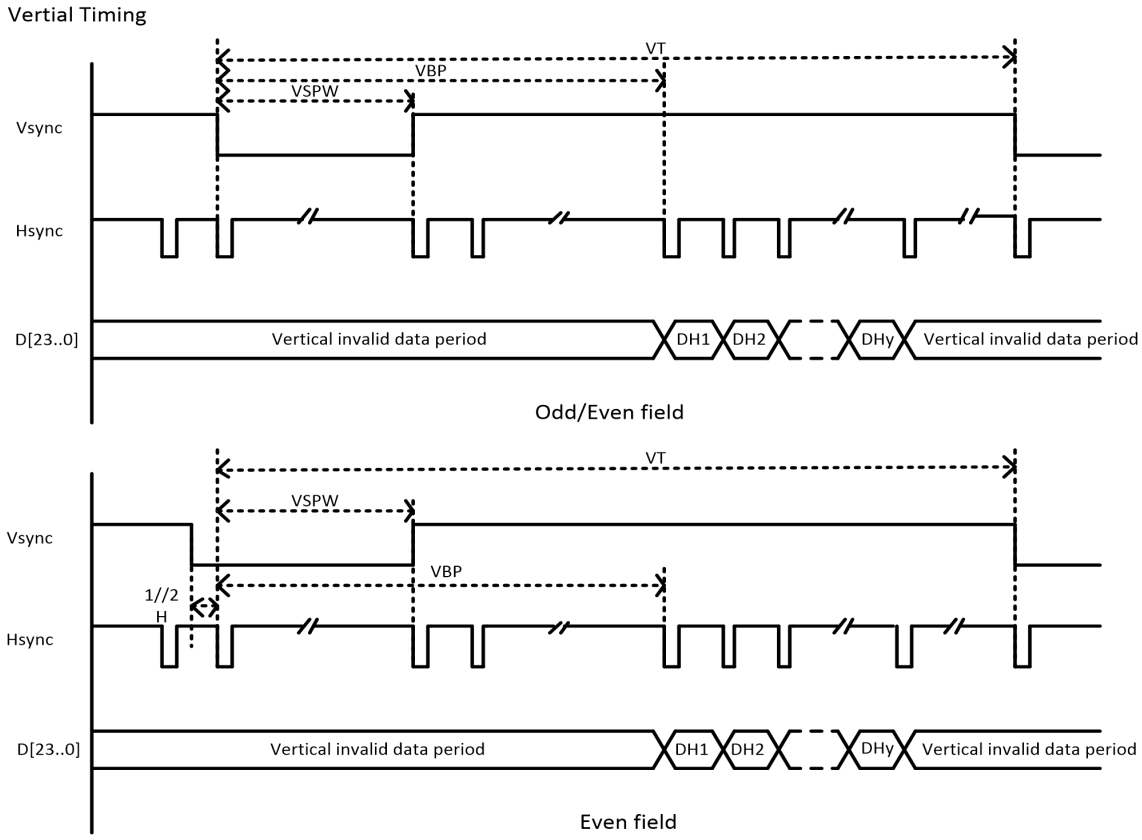
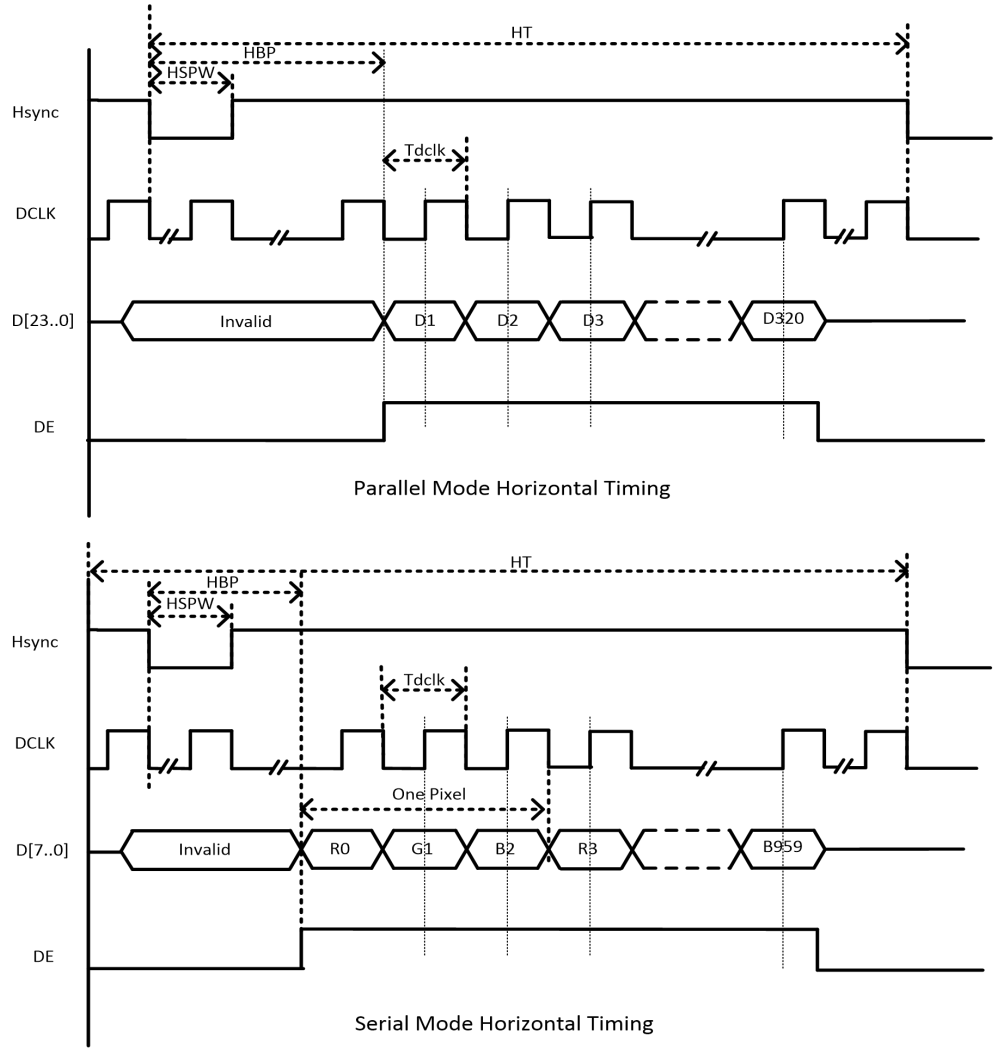
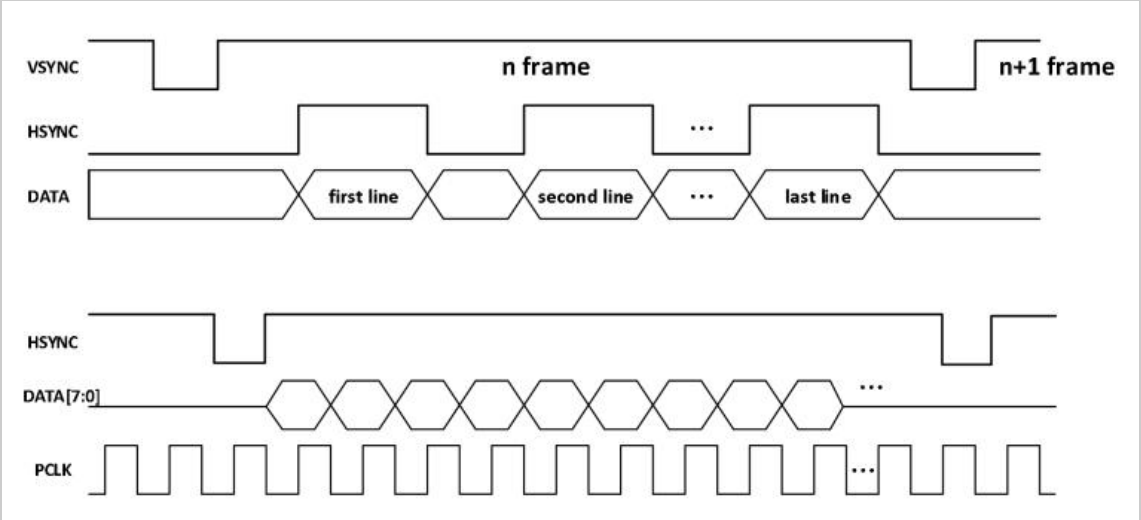


Figure 6-3 HV Interface Horizontal Timing



6.3.3.5 DC (Digital Camera) Interface (Only for TCON_LCD0)

Figure 6-46-5 DC Interface Timing



6.3.3.6 BT.656 Interface (Only for TCON_LCD0)

When the data in YUV format is transmitted in HV mode, TCON_LCD0 needs to use ITU-R BT.656 protocol. Compared with standard CSI interface, there are not synchronous signals, such as FIELD, VSYN, and HSYN, for BT.656 interface. The horizontal and vertical synchronization information of images are built in the BT.656 data stream. BT.656 data format only includes PCLK signal, DVLD signal (unnecessary), and data bus signal. The BT.656 protocol provides 8-bit width and interlaced data of YUV422 format. The encoding format for each line is as follows:

Line=End of Active Video (EAV) + horizontal blanking data (80H/10H) + Start of Active Video (SAV) + valid data (UYVY)

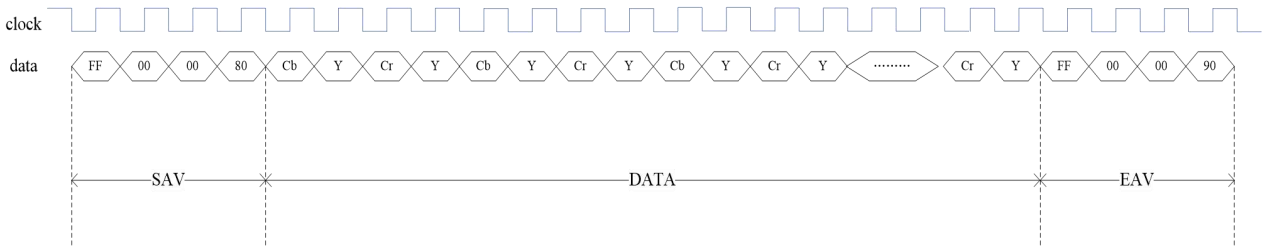
Both of EAV and SAV consist of a 4-bytes sequence in the following format: FF 00 00 XY. The first three bytes are fixed as hexadecimal 8'hFF 8'h00 8'h00. The fourth byte of XY is used to control the format. The assignment of the XY bit is shown in the following table.

Table 6-10 Analysis of XY Signal

BIT	7	6	5	4	3	2	1	0
XY	1'b1	F	V	H	P3	P2	P1	P0
F	0: during field 1 1: during field 2							
V	1: during field blanking 0: field active							
H	0: in SAV 1: in EAV							
P3-P0	protection bits. Single channel: P3=V^H，P2=F^H，P1=F^V，P0=F^V^H Multi-Channel: Channel ID							

During single-channel data transmission, P3-P0 is used for calibration. The transmission timing is shown in the following figure.

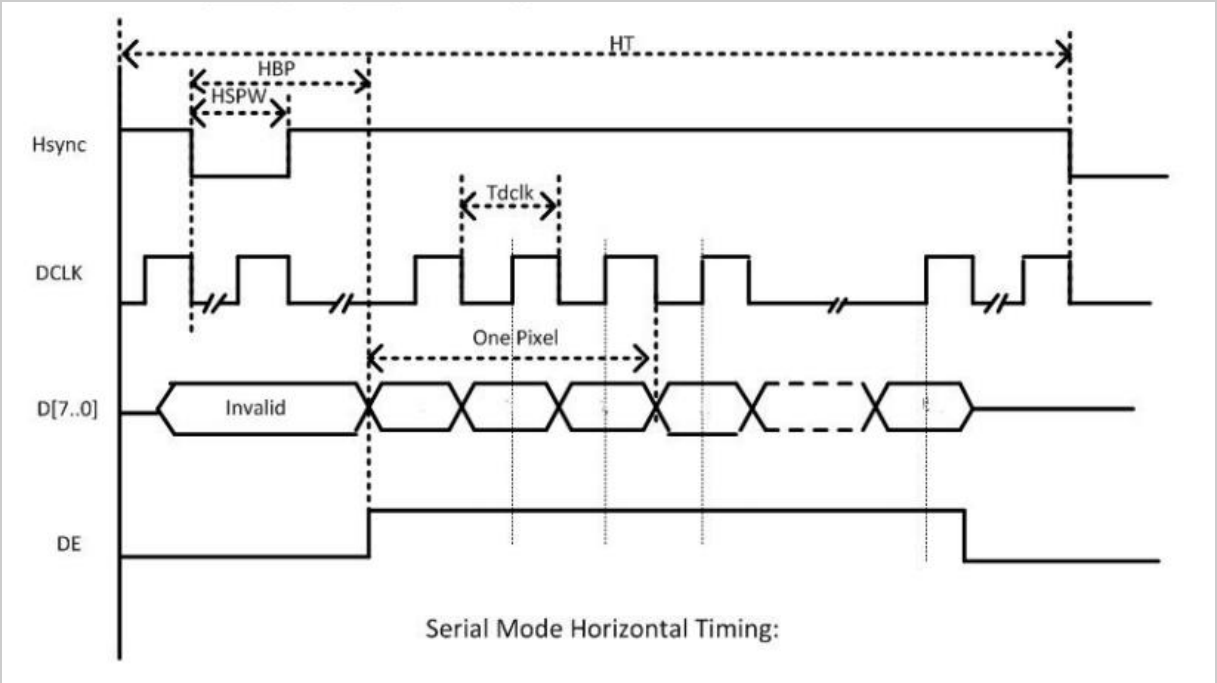
Figure 6-6 Singl-channel Transmission Timing



In programming, the final output format is finished in rgb2yuv, which means the 8-bit data format output by rgb2yuv is the format shown above. ctrl_data_out just inplement the pin-mapping of the data.

6.3.3.7 BT.601 Interface (Only for TCON_LCD0)

Figure 6-7 BT.601 Interface Timing



6.3.3.8 i8080 Interface (Only for TCON_LCD0)

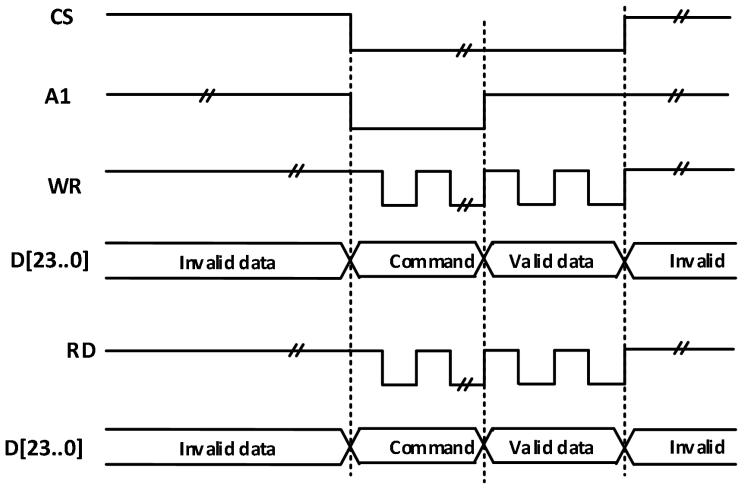
The i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels. The CPU control signals are active low.

Table 6-11 CPU Panel Signals

Signal Name	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure relationship between basic timing and CPU timing. WR is 180o delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 is set by “LCD_CPUI/F”.

Figure 6-8 i8080 Interface Timing



When CPU I/F is in IDLE state, it can generate WR/RD timing by setting “Lcd_CPUI/F”. The CS strobe is one DCLK width, and the WR/RD strobe is half DCLK width.

6.3.3.9 LVDS Interface (Only for TCON_LCD0)

Table 6-12 LVDS Panel Signals

Signal Name	Description	Type
CKP	The positive port of clock	O
CKN	The negative port of clock	O
D0P	The positive port of data channel 0	O
D0N	The negative port of data channel 0	O
D1P	The positive port of data channel 1	O
D1N	The negative port of data channel 1	O
D2P	The positive port of data channel 2	O
D2N	The negative port of data channel 2	O
D3P	The positive port of data channel 3	O
D3N	The negative port of data channel 3	O

NOTE

A523 adopts 7:1 LVDS interface.

The following figures show the timing of LVDS interface.

Figure 6-9 LVDS Single Link JEDIA Mode Interface Timing

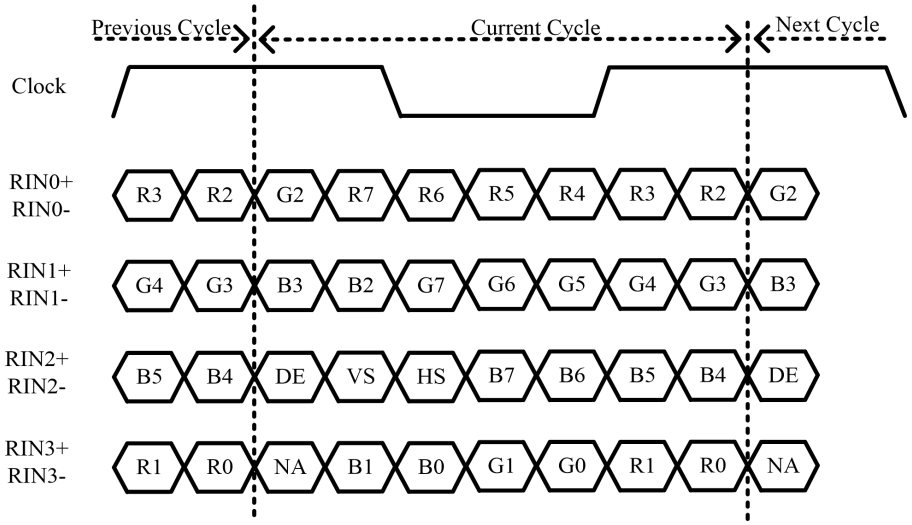
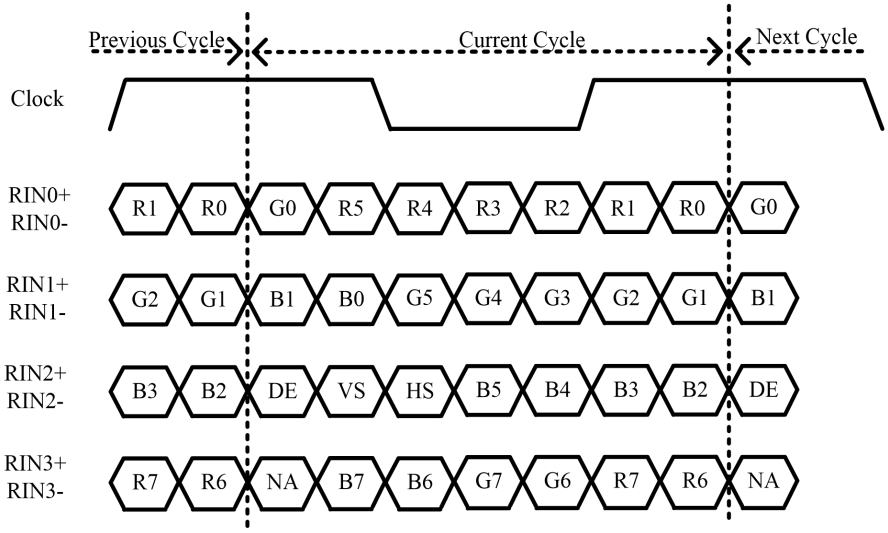
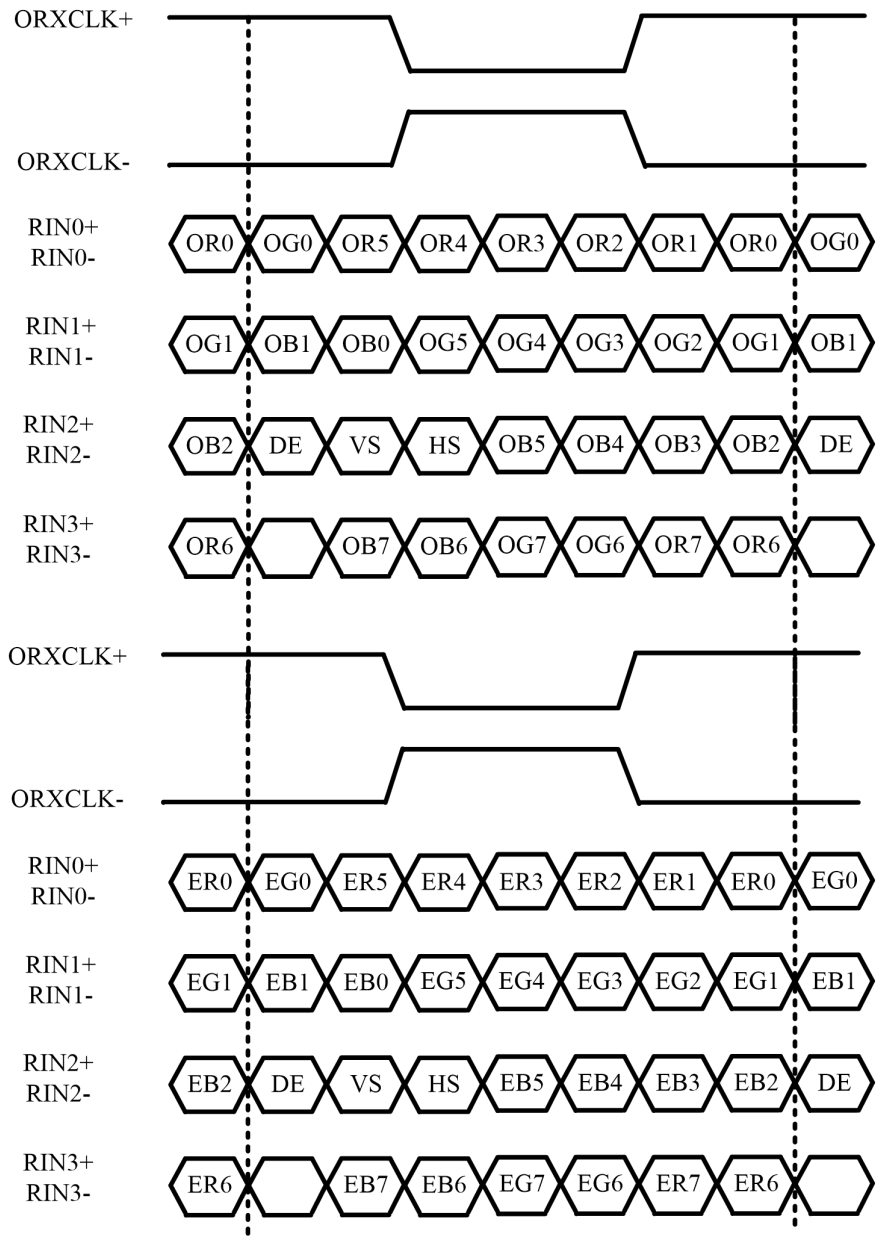


Figure 6-10 LVDS single link NS Mode interface timing



The following figure shows the timing of one mode of the dual-link LVDS, in which odd pixel channel and even pixel channel output to a single-monitor. Dual-link can be configured in the LVDS_DUAL_CHANEL_SRC_SEL bit (bit [30]) of LCD_LVDS_ANA0_REG register.

Figure 6-11 LVDS Dual Link NS Mode Interface Timing



6.3.3.10 CEU Module (Only for TCON_LCD0)

This module enhances color data from DE .

R′ = Rr*R + Rg*G + Rb*B + Rc

G′ = Gr*R + Gg*G + Gb*B + Gc

B′ = Br*R + Bg*G + Bb*B + Bc

Rr, Rg, Rb, Gr, Gg, Gb, Br, Bg, Bb s13 (-16, 16)

Rc, Gc, Bc	s19 (-16384, 16384)
R, G, B	u8 [0-255]

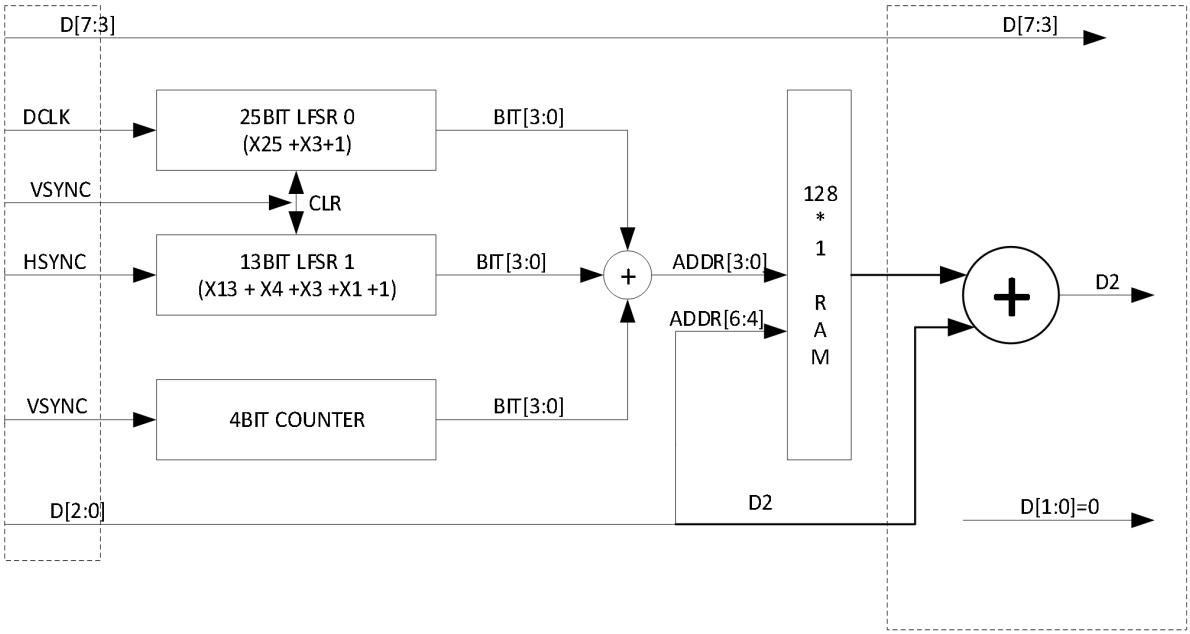
R′ has the range of [Rmin, Rmax]

G′ has the range of [Rmin, Rmax]

B′ has the range of [Rmin, Rmax]

6.3.3.11 FRM Module (Only for TCON_LCD0)

Figure 6-12 FRM Module

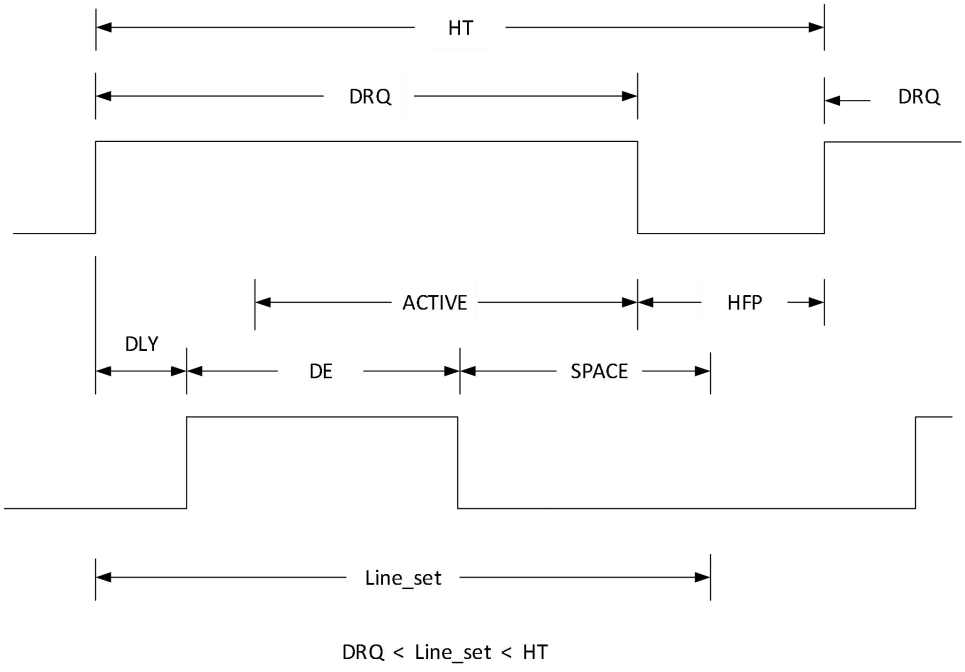


6.3.3.12 MIPI DSI Notes

The requirements on MIPI DSI mode are as follows.

- When using MIPI DSI as display interface, the data clk of TCON needs be started firstly.
- When it is used with DSI video mode, the setting of block space needs to meet the following relationship.

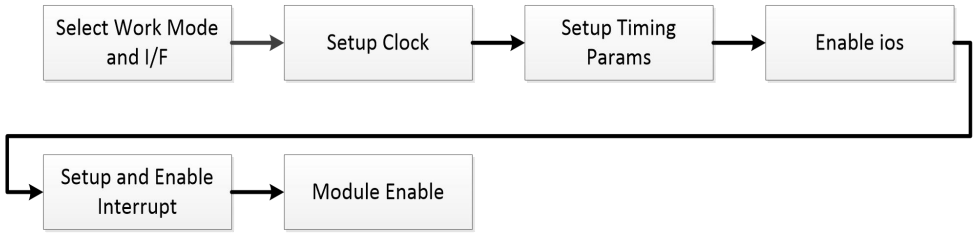
Figure 6-13 The Data Timing of MIPI DSI Video Mode



6.3.4 Programming Guidelines (Only for TCON_LCD0)

6.3.4.1 Enabling HV Mode

Figure 6-14 HV Mode Initial Process



Parallel RGB

Step 1 Select HV interface type

Configure LCD_CTL_REG[LCD_IF] (reg0x40) to 0 to select HV (Sync+DE) mode, and configure LCD_HV_IF_REG[HV_MODE] (reg0x58) to 0 to select 24bit/1cycle parallel mode.

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = 24bit/1cycle parallel mode;

Step 2 Clock configuration

NOTE

- In parallel RGB mode, the displayed pixel clock (pixel_CLK) is required to be consistent with the DCLK, the pixel_clk(pixel_clk=Ht*Vt*frame rate) is decided by external LCD.
- When using phase adjustment function, the LCD_IO_POL_REG.DCLK_SEL (reg0x88) selects dclk0–2 of different phase, and LCD_IO_POL_REG.IO2_INV can achieve 180°phase delay.

Configure corresponding frequency by setting PLL_VIDEO0/1 register, and configure TCON LCD0 Clock register.

Configure internal frequency division of TCON_LCD. Based on clock source of TCON and DCLK clock ratio, configure LCD_DCLK_REG[LCD_DCLK_DIV]. If using phase adjustment function, LCD_DCLK_REG[LCD_DCLK_EN] needs be set, usually is 0xf. When the dclk1 and dclk2 in LCD_DCLK_REG[LCD_DCLK_EN] are used, the value of LCD_DCLK_REG[LCD_DCLK_DIV] needs no less than 6.

lcd_dev[sel]->lcd_dclk.dclk_en = en;

lcd_dev[sel]->lcd_dclk.dclk_div = div;

Step 3 Set sequence parameters

The sequence parameters include x,ht,hbp,hspw,y,vt,vbp,vspw, and correspond to LCD_BASE_REG from reg0x48 to reg 0x54. Note that hbp includes hspw, and vbp includes vspw. And LCD_BASIC2_REG.VT needs be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic0.x = x-1;

lcd_dev[sel]->lcd_basic0.y = y-1;

lcd_dev[sel]->lcd_basic1.ht = ht-1;

lcd_dev[sel]->lcd_basic1.hbp = hbp-1;

lcd_dev[sel]->lcd_basic2.vt = vt*2;

lcd_dev[sel]->lcd_basic2.vbp = vbp-1;

lcd_dev[sel]->lcd_basic3.hspw = hspw-1;

lcd_dev[sel]->lcd_basic3.vspw = vspw-1;

Step 4 Open IO output

Set the corresponding data IO enable and control signal IO enable of LCD_IO_TRI_REG (reg0x8C) to 0 to start enable. Note that except the internal IO of TCON_LCD, the external GPIO mapping needs to be set to LCD mode.

When some control signals require polarity reversal, it can realize by setting LCD_IO_POL_REG.IO0-3_INV (reg0x88).

Step 5 Set and open interrupt function

The LCD_GINT0_REG (reg0x4) controls interrupt mode and flag, and the LCD_GINT1_REG (reg0x8) sets the interrupt line position of Line interrupt mode.

V interrupt:

lcd_dev[sel]->lcd_gint0.vb_en = 1;

Line interrupt:

lcd_dev[sel]->lcd_gint1.lcd_line_int_num = line;

lcd_dev[sel]->lcd_gint0.line_en = 1;

Step 6 Open module enable

Enable LCD_CTL_REG.LCD_EN (reg0x40) and LCD_GCTL_REG.LCD_EN (reg0x00).

lcd_dev[sel]->lcd_ctl.lcd_en = 1;

lcd_dev[sel]->lcd_gctl.lcd_en = 1;

The following table is an example of typical parameter configuration.

Table 6-13 HV Mode Configuration Example

Step	Register	Typical Value of Simulation	Description
1	LCD_HV_IF_REG (0x0058)	32'h0000_0000	Select parallel RGB
	LCD_CTL_REG (0x0040)	32'h0000_0041	Select HV (Sync+DE) mode
	/	/	Enable some functions such as 3DFIFO and FRM. (Optional)
2	LCD_DCLK_REG (0x0044)	32'hf000_0002	/
3	LCD_BASIC0_REG (0x0048)	32'h0063_000f	Set x and y.
	LCD_BASIC1_REG (0x004C)	32'h0095_0013	Set ht and hbp.
	LCD_BASIC2_REG (0x0050)	32'h0030_0001	Set vt and vbp.
	LCD_BASIC3_REG (0x0054)	32'h0009_0000	Set HSPW and VSPW to get the configured value. The actule value is equal to the configured value plus one.
4	LCD_IO_POL_REG (0x0088)	32'h0000_0000	/
	LCD_IO_TRI_REG (0x008C)	32'he000_0000	1: Disable 0: Enable
5	LCD_GINT1_REG (0x008)	32'h0010_0000	/
	LCD_GINT0_REG (0x004)	32'h2000_0000	/

Step	Register	Typical Value of Simulation	Description
6	LCD_CTL_REG (0x0040)	32'h8000_0041	Open module enable.
	LCD_GCTL_REG (0x0000)	32'h8000_0000	Enable vs and hs to count.

Serial RGB

The serial RGB mode is consistent with parallel RGB mode, the main difference is the definition of clock and the sequence of serial data. The difference is as follows.

Step 1 Select HV interface type

Set LCD_CTL_REG.LCD_IF (reg0x40) to 0 to select HV(Sync+DE) mode; set LCD_HV_IF_REG.HV_MODE (reg0x58) to select 8bit/3cycle RGB serial mode (RGB888), 8bit/4cycle Dummy RGB mode (DRGB) or 8bit/4cycle RGB Dummy mode (RGBD).

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = Serial mode;

Step 2,3 Set clock and sequence parameters

In serial RGB mode, DCLK is the transfer clock of each byte data. In the same resolution, pixel_clk of serial RGB is three times of its clock in parallel RGB, and ht,hbp,hspw own the same conversion relation. When display is split into odd field and even field, LCD_BASIC2_REG.VT needs not to be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic2.vt = vt;

Set LCD_HV_IF_REG.RGB888_ODD_ORDER/LCD_HV_IF_REG.RGB888_ODD_EVEN to select RGB output sequence of the selected odd and even lines.

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_even = seq_even;

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_odd = seq_odd;

6.3.4.2 Enabling DC Mode

The DC mode configuration process is similar to the parallel mode of HV mode.

6.3.4.3 Enabling BT.656 Mode

The BT.656 mode configuration process is similar to the parallel mode of HV mode. The following table is an example of typical parameter configuration.

Table 6-14 BT.656 Mode Configuration Example

Step	Register	Typical Value of Simulation	Description
1	LCD_HV_IF_REG (0x0058)	32'h0000_0000	Select parallel RGB

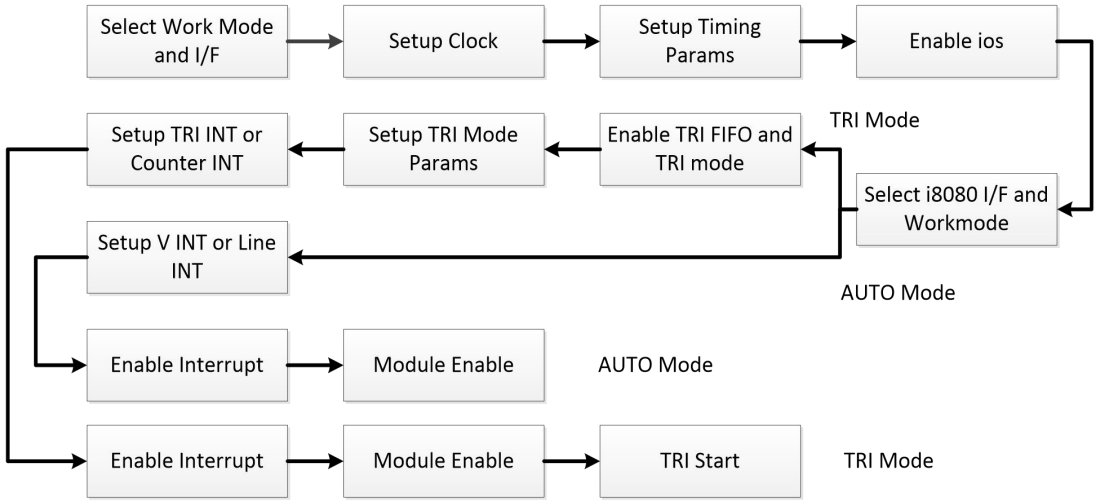
Step	Register	Typical Value of Simulation	Description
	LCD_CTL_REG (0x0040)	32'h0000_0041	Select HV (Sync+DE) mode
	/	/	Enable some functions such as 3DFIFO and FRM. (Optional)
2	LCD_DCLK_REG (0x0044)	32'hf000_0002	/
3	LCD_BASIC0_REG (0x0048)	32'h0063_000f	Set x and y.
	LCD_BASIC1_REG (0x004C)	32'h0095_0013	Set ht and hbp.
	LCD_BASIC2_REG (0x0050)	32'h0030_0001	Set vt and vbp.
	LCD_BASIC3_REG (0x0054)	32'h0009_0000	Set HSPW and VSPW to get the configured value. The actule value is equal to the configured value plus one.
4	LCD_IO_POL_REG (0x0088)	32'h0000_0000	/
	LCD_IO_TRI_REG (0x008C)	32'he000_0000	1: Disable 0: Enable
5	LCD_GINT1_REG (0x008)	32'h0010_0000	/
	LCD_GINT0_REG (0x004)	32'h2000_0000	/
6	LCD_CTL_REG (0x0040)	32'h8000_0041	Open module enable.
	LCD_GCTL_REG (0x0000)	32'h8000_0000	Enable vs and hs to count.

6.3.4.4 Enabling BT.601 Mode

The BT.601 mode configuration process is similar to the parallel mode of HV mode.

6.3.4.5 Enabling i8080 Mode

Figure 6-15 i8080 Mode Initial Process



Step 1 Select i8080 interface type.

Step 2 The step is the same as HV mode, but pulse adjustment function is invalid.

Step 3 The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode, or a handful of functions such as CMAP will not be able to apply.

Step 4 The step is the same as HV mode.

Step 5 Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------If For TRI mode----------

Step 6 Open TRI FIFO switch, and TRI mode function.

Step 7 Set parameters of TRI mode, including block size, block space and block number.

NOTE

- When output interface is parallel mode, then the setting value of block space parameter is not less than 20.
- When output interface is 2 cycle serial mode, then the setting value of block space parameter is not less than 40.
- When output interface is 3 cycle serial mode, then the setting value of block space parameter is not less than 60.
- When output interface is 4 cycle serial mode, then the setting value of block space parameter is not less than 80.

Step 8 Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 0x8C register is set to "1", to open up input of pad.

Step 9 Open the total switch of interrupt.

Step 10 Open the total enable of interrupt.

Step 11 Operate “tri start” operation (the bit1 of LCD_CPU_IF_REG is set to "1").

----------**If For Auto mode**----------

Step 6 Set and open V interrupt or Line interrupt, the step is the same as HV mode.

Step 7 Open module total enable.

6.3.5 Register List

Module Name	Base Address
TCON_LCD0	0x0550 1000
TCON_LCD1	0x0550 2000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x0014+N*0x04(N=0-5)	LCD FRM Seed Register
LCD_FRM_TAB_REG	0x002C+N*0x04(N=0-3)	LCD FRM Table Register
LCD_3D_FIFO_REG	0x003C	LCD 3D Fifo Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register
LCD_CPU_WR_REG	0x0064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x0068	LCD CPU Panel Read Data Register0

