7 Video Input Interfaces

7.1 CSIC

7.1.1 Overview

The CMOS Sensor Interface Controller (CSIC) is an image or video data receiver, which can receive image or video data via camera interface and store the data in memory directly.

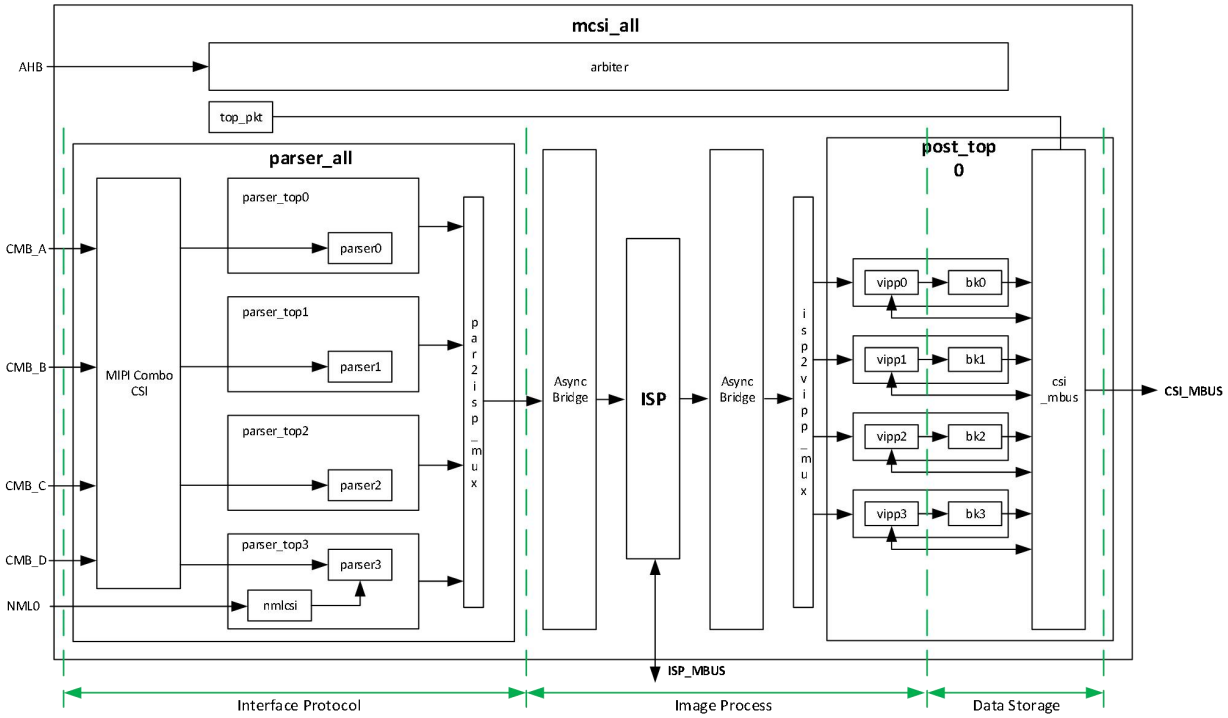
The CSIC includes the following features:

- MIPI CSI supports the following
  - 8M@30fps RAW12 2F-WDR, size up to 3264(H) x 2448(V)
  - 4+ 4-lane, 4+2+2-lane, or 2+2+2+2-lane MIPI Interface
    - MIPI CSI2 V1.1
    - MIPI DPHY V1.1
    - 2.0 Gbit/s per lane
  - Crop function
  - Frame-rate decreasing via software
- Parallel CSI supports the following
  - 16-bit digital camera interface
  - 8/10/12/16-bit width
  - BT.656, BT.601, BT.1120 interface
  - Dual Data Rate (DDR) sample mode with pixel clock up to 148.5MHz
  - ITU-R BT.656 up to 4*720P@30fps
  - TU-R BT.1120 up to 4*1080P@30fps
- BK supports the following:
  - 4-lane BK and BK0-3 supports 4-lane time-multiplexing
  - 4 DMA controllers for 4 video stream storage
    - Conversion of interlaced input to progressive output
    - Data conversion supports: YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
    - Horizontal and vertical flip
- BK doesn’t support anti-aliasing and noise reduction

7.1.2 Block Diagram

The following figure shows block diagram of the CSIC.

Figure 7-1 CSIC Block Diagram



7.1.3 Functional Description

7.1.3.1 External Signals

Table 7-1 CSIC External Signals

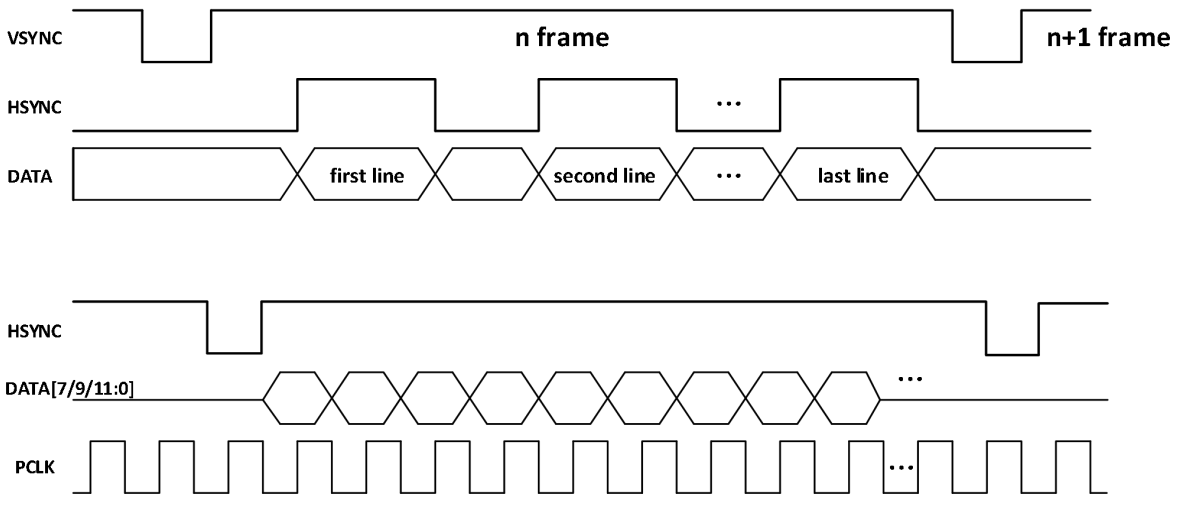
Signal Name	Description	Type
MIPI CSI		
MCSIA-D0N	MIPI CSI Controller A Data0 Negative Signal	AI
MCSIA-D0P	MIPI CSI Controller A Data0 Positive Signal	AI
MCSIA-D1N	MIPI CSI Controller A Data1 Negative Signal	AI
MCSIA-D1P	MIPI CSI Controller A Data1 Positive Signal	AI
MCSIA-CKN	MIPI CSI Controller A Clock Negative Signal	AI
MCSIA-CKP	MIPI CSI Controller A Clock Positive Signal	AI
MCSI0-MCLK	Master Clock for MIPI Sensor	O
MCSIB-D0N	MIPI CSI Controller B Data0 Negative Signal	AI
MCSIB-D0P	MIPI CSI Controller B Data0 Positive Signal	AI
MCSIB-D1N	MIPI CSI Controller B Data1 Negative Signal	AI
MCSIB-D1P	MIPI CSI Controller B Data1 Positive Signal	AI
MCSIB-CKN	MIPI CSI Controller B Clock Negative Signal	AI
MCSIB-CKP	MIPI CSI Controller B Clock Positive Signal	AI

Signal Name	Description	Type
MCSI1-MCLK	Master Clock for MIPI Sensor	O
MCSIC-D0N	MIPI CSI Controller C Data0 Negative Signal	AI
MCSIC-D0P	MIPI CSI Controller C Data0 Positive Signal	AI
MCSIC-D1N	MIPI CSI Controller C Data1 Negative Signal	AI
MCSIC-D1P	MIPI CSI Controller C Data1 Positive Signal	AI
MCSIC-CKN	MIPI CSI Controller C Clock Negative Signal	AI
MCSIC-CKP	MIPI CSI Controller C Clock Positive Signal	AI
MCSI2-MCLK	Master Clock for MIPI Sensor	O
MCSID-D0N	MIPI CSI Controller D Data0 Negative Signal	AI
MCSID-D0P	MIPI CSI Controller D Data0 Positive Signal	AI
MCSID-D1N	MIPI CSI Controller D Data1 Negative Signal	AI
MCSID-D1P	MIPI CSI Controller D Data1 Positive Signal	AI
MCSID-CKN	MIPI CSI Controller D Clock Negative Signal	AI
MCSID-CKP	MIPI CSI Controller D Clock Positive Signal	AI
MCSI3-MCLK	Master Clock for MIPI Sensor	O
CSI-SM-HS	MIPI CSI Slave Mode Horizontal SYNC	O
CSI-SM-VS	MIPI CSI Slave Mode Vertical SYNC	O
Parallel CSI		
NCSI-PCLK	Parallel CSI Pixel Clock	I
NCSI-MCLK	Parallel CSI Master Clock	O
NCSI-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI-D[15:0]	Parallel CSI Data Bit	I

7.1.3.2 CSIC Input Timing

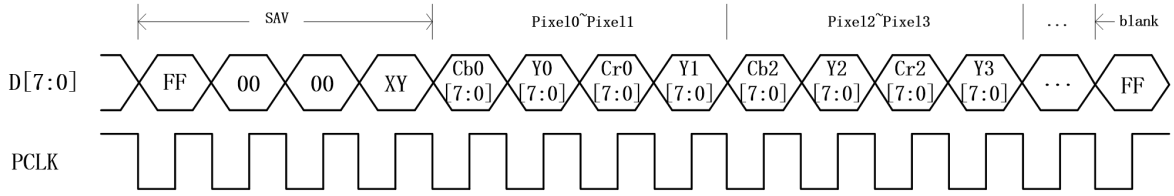
The following figure shows the timing of 8bit CMOS Sensor Interface, in this figure clock active at the rising edge, VSYNC valid at positive, HSYNC valid at positive.

Figure 7-2 8-bit DC Sensor Interface Timing



The following figure shows the timing of 8-bit YCbCr4:2:2 with embedded syncs (BT.656).

Figure 7-3 8-bit YCbCr4:2:2 with Embedded Syncs (BT.656)



The following table shows the header code of BT.656.

Table 7-2 BT.656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[7] (MSB)	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

The following table shows the Header Data Bit Definition of BT.656.

Table 7-3 BT.656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

7.1.3.3 CSIC FIFO Distribution

Table 7-4 CSIC FIFO Distribution

Input format	YUV422/YUV420		Raw
Output format	Planar	UV combined	Raw
FIFO0	Y	Y	All pixels data
FIFO1	Cb (U)	CbCr (UV)	-
FIFO2	Cr (V)	-	-

7.1.3.4 Pixel Format Arrangement

The following figures show the Pixel Format Arrangement.

Figure 7-4 RAW-8 Format

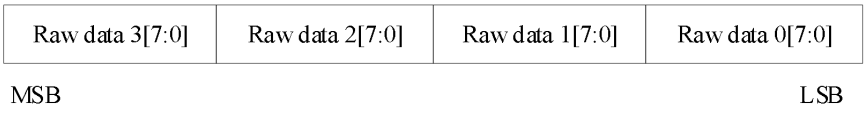


Figure 7-5 Y Format

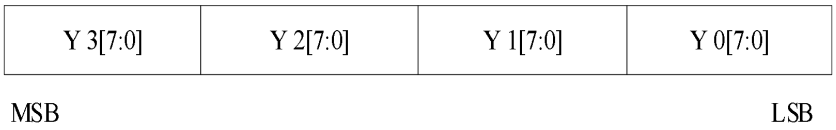
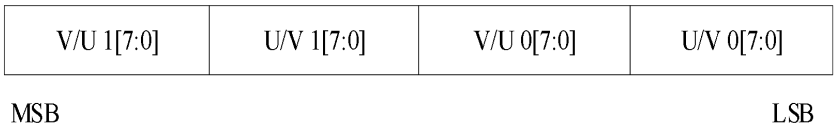


Figure 7-6 UV-Combined Format



7.1.3.5 Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

- For YUV422 format, pixel unit is a YU/YV combination.
- For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
- For Bayer and RAW format, pixel unit is a R/G/B single component.

7.1.3.6 Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of Y0U0Y1V1 will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of Y1U0Y0V1 will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

7.1.4 Programming Guidelines

7.1.4.1 Key Points for Async Bridge Configuration

- If ISP uses work clock with lower frequency than that of parser and post.

Step 1 Configure the field ISP_BRIDGE_EN (bit [3]) of CSIC_TOP_EN_REG as 1'b1 to enable async bridge

Step 2 Configure the field MCSI_PARSER_CLK_MODE (bit [0]) of CCU_CLK_MODE_REG as 1'b1 to make CSI parser work in CSI clock.

Step 3 Configure the field MCSI_POST_CLK_MODE (bit [1]) of CCU_CLK_MODE_REG as 1'b1 to make CSI post work in CSI clock.

- If ISP uses work clock with the same frequency as parser and post

Step 1 Configure the field ISP_BRIDGE_EN (bit [3]) of CSIC_TOP_EN_REG as 1'b0 to disable and bypass async bridge.

Step 2 Configure the field MCSI_PARSER_CLK_MODE (bit [0]) of CCU_CLK_MODE_REG as 1'b0 to make CSI parser work in ISP core clock.

Step 3 Configure the field MCSI_POST_CLK_MODE (bit [1]) of CCU_CLK_MODE_REG as 1'b0 to make CSI post work in ISP core clock.

7.1.4.2 Configuration Notes

- The CCU_CLK_GATING_DISABLE bit (bit [31]) of CCU_CLK_MODE_REG register is configured as 0 by default, that is, the clock in CSIC CCU is gated off by default.
- The MCSI_POST_CLK_MODE bit (bit [1]) and MCSI_PARSER_CLK_MODE bit (bit [0]) of CCU_CLK_MODE_REG register are configured as 1 by default, that is, CSI post and CSI parser work in CSI clock by default.
- The sequence of CSI reset, CSIC clock enable, and PPU power-on is as follows:

  CSIC reset -> PPU power-on -> CSIC clock enable (including: ISP_Clock, CSI Clock, ISP MCLK, CSI MCLK, CSI BUS GATING, and CSI Master0/1/2/3 Clock)

- There are two soft reset bits for MBUS:

Table 7-5 Soft Reset bits for MBUS

Bits	Regsiters	Description
MISP_MBUS_RST (bit [8], high active)	CCU_ISP_CLK_EN_REG	Reset the MBUS interface logic circuit in ISP.
MCSI_POST0_MBUS_RST (bit [20], high active)	CSIC_CCU_POST0_CLK_EN_REG	Reset the MBUS interface logic circuit in POST0.